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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER

MARIAM, DANIEL G

ART UNIT	PAPER NUMBER
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2625

DATE MAILED: 01/25/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/801,401

Applicant(s)

PINE, JOSHUA I.

Examiner

DANIEL G. MARIAM

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 12 May 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-4, 6-10 and 23-31 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-4, 6-10, and 23-31 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

Response to Arguments

1. Applicant's arguments filed on May 12, 2005 have been fully considered but they are not deemed to be persuasive. For at least the following reasons.

Applicant argues starting on page 9 of the remarks, that the secondary reference to Schoenzeit does not disclose storing one or more image data awaiting additional processing by the imaging system. Specifically, applicant alleges that items 40a-40c are output device control modules for managing and sending rasterized image data to output devices 16, such as an image recorder. Accordingly, items 40a-40c do not store one or more image data awaiting additional image processing by the imaging system. The Examiner disagrees. First, raster image processor (RIP) is provided in each of the above identified modules 40a-40c so as to generate raster image data for the images contained in the graphic image files stored in the associated RIP queues (See for example, col. 5, lines 53-60). Second, at col. 11, lines 11-14, Schoenzeit states: "a first queue for storing graphic image files to be processed by the associated output device; the graphic image files stored in the first queue containing data for different images in a first order; means for rasterizing image data from the graphic image files stored in the first queue to provide raster image data for a plurality of images; a second queue for storing the raster image data generated by the rasterizing means; and means for selecting the image data from the graphic image files stored in the first queue on a real-time basis for processing by the rasterizing means, the selecting means being responsive to parameters of the graphic image files and the associated output device to manage the flow of image data from said first queue to the rasterizing means and from the rasterizing means to the associated output device via said second queue; such that the "*rasterizer means can process additional image data from the graphic image files stored in said first queue*

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even while said associated output device cannot receive additional data from the second queue."

Thus, Schoenzeit does disclose storing one or more image data awaiting additional processing by the imaging system.

Applicant further argues on page 9 of the remarks, that Telle fails to disclose, teach or suggest "an intermediate storage queue configured to store one or more processed intermediate image data, wherein the intermediate storage queue is communicatively coupled to the image processing circuitry and the transformation circuitry," as recited in amended claim 1. The Examiner disagrees. Given the broadest reasonable interpretation, the image processing and the transformation circuitry are done by a single digital image processor of Telle as shown at item 52, in Fig. 2, and the buffer shown at item 60 and/or 56 in Fig. 2 does indeed store a processed intermediate image data. Thus, Telle in combination with Schoenzeit meet applicant's claimed invention. Please note, to avoid the primary reference (Telle) as a prior art, applicant should amend the claim by including limitations that identify the image processing circuitry and the transformation circuitry as two separate circuitries.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 1-4, 6-10 and 23-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Telle (6,469,801) in view of Schoenzeit, et al. (5,619,624).

With regard to claim 1, Telle discloses an imaging system (See for example, Fig. 2) comprising: an image sensing circuitry that produces a raw image data (See item 50, in Fig. 2); an image processing circuitry, i.e., digital image processing, communicatively coupled to the image sensing circuitry, that processes the raw image data into a processed intermediate image data (See item 52, in Fig. 2); a transformation circuitry (which also corresponds to the digital image processing) communicatively coupled to the image processing circuitry, that transforms the processed intermediate image data (the digital image processor does perform, among other things, a scaling operation, which generally is a transformation of an image from one size to another, such as enlarging or reducing) into a processed final image data (See for example item 52, in Fig. 2; and col. 5, lines 26-50); a communication circuitry, communicatively coupled to the transformation circuitry, that links the imaging system to a final storage (See for example, item 56, in Fig. 2; and item 30, in Fig. 2); an intermediate storage queue, i.e., buffer, configured to store one or more processed intermediate image data, wherein the intermediate storage queue is communicatively coupled to the image processing circuitry and the transformation circuitry (See for example, item 60 and/or 56, and item 52 in Fig. 2); and the intermediate storage queue storing the one or more processed intermediate image data from the image processing circuitry (awaiting additional image processing) by the transformation circuitry, i.e., digital image processing, (See for example, col. 4, lines 12-34, and item 52, in Fig. 2).

Telle does not expressly call for storing one or more image data awaiting additional processing by the imaging system. However, Schoenzeit, et al. (See for example, items 40a-40c; and col. 11, lines 11-14. Also, argument presented above in paragraph 1 is not repeated herein, but is incorporated by reference) teaches this feature. Therefore, it would have been obvious to

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one having ordinary skill in the art to incorporate the teaching as taught by Schoenzeit, et al. into the system of Telle if no other reason than to store image data or files awaiting additional processing by the system, and to do so would at least provide efficient storing and processing of a large amount of data in a timely manner.

With regard to claim 2, the imaging system of claim 1 wherein the intermediate storage queue is communicatively coupled to the image sensing circuitry and stores one or more raw image data, the one or more raw image data being delivered to the image processing circuitry upon the occurrence of an event (See item 60 and/or 54, in Fig.2).

With regard to claim 3, the imaging system of claim 2, wherein the one or more raw image data is held in the intermediate storage queue while the image processing circuitry is processing another image data, and one of the one or more raw image data is delivered to the image processing circuitry when the image processing circuitry ceases processing on the another image data (See for example, image data provided by the user block item 30 to the digital image processor while the raw image data is stored in item 54 as illustrated in Fig. 2; and col. 8, lines 5-25).

With regard to claim 4, the imaging system of claim 2 wherein additional raw image data are stored in the intermediate storage queue, and each of the raw image data stored in the intermediate storage queue are delivered to the image processing circuitry when the amount of raw image data in the intermediate storage queue reaches a predetermined level (broadly reads on col. 4, line 43 through col. 5, line 19; particularly, col. 5, lines 14-19).

With regard to claim 6, the imaging system of claim 1 wherein the one or more processed intermediate image data is held in the intermediate storage queue while the

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transformation circuitry is processing another processed intermediate image data, and one of the one or more processed intermediate image data is delivered to the transformation circuitry when the transformation circuitry ceases processing on the another processed intermediate image data (See for example, item 60, in Fig.2).

With regard to claim 7, the imaging system of claim 1 wherein additional processed intermediate image data are stored in the intermediate storage queue, and each of the processed intermediate image data stored in the intermediate storage queue are delivered to the transformation circuitry when the amount of processed intermediate image data in the intermediate storage queue reaches a predetermined level (which broadly reads on col. 5, lines 14-19 and lines 26-50; and item 60, in Fig.2).

With regard to claim 8, the imaging system of claim 1 wherein the transformation circuitry performs a compression (this feature is also embedded in the digital image processor) on the image data (See for example, col. 4, lines 51-66).

With regard to claim 9, the imaging system of claim 1 further comprises a processing circuitry monitoring the status of the intermediate storage queue (See for example, item 46 or 60, in Fig. 2).

With regard to claim 10, the imaging system of claim 1, wherein the imaging system processes the image data in the intermediate storage queue in response to an indication that the imaging system has been linked to an external power source (See Fig. 2).

Claims 23, 24, 25, 26, 27, 28, 29, 30 and 31 are rejected the same as claims 1, 2, 3, 4, 6, 7, 8, 9, and 10 respectively except claims 23, 24, 25, 26, 27, 28, 29, 30 and 31 are method

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claims. Thus, arguments analogous to those presented above for claims 1, 2, 3, 4, 6, 7, 8, 9, and 10 are respectively applicable to claims 23, 24, 25, 26, 27, 28, 29, 30 and 31.

Conclusion

4. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DANIEL G. MARIAM whose telephone number is 571-272-7394. The examiner can normally be reached on M-F (7:00-4:30) FIRST FRIDAY OFF.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, BHAVESH M. MEHTA can be reached on 571-272-7453. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

July 19, 2005


DANIEL MIRIAM
PRIMARY EXAMINER